REMARKS

In the Office Action mailed March 25, 2004, claim 1-18 were rejected. Claims 3-11, 16-17, and 19-23 have been canceled. Claims 10 have been withdrawn. Claims 1 and 14 have been amended. Applicant reserves the right to resume prosecution of all claims as originally filed. Claims 25-30 are new. Claims 1, 2, 12-15, and 24-30 are pending.

In the following, the Examiner's comments are included in bold, indented type, followed by the Applicant's remarks:

> **2. The Information Disclosure Statement filed November 16, 2001 fails to comply with the provisions of MPEP § 609 because copies of the cited references have not been provided. In fact, the cover letter for the information disclosure statement admits that copies of the cited references have not been provided and are instead found in a list of other application numbers. Applicant is reminded of the provisions of 37 CFR 1.98(d) which states:**
>
> **"(d) A copy of any patent, publication, pending U.S. application or other information, as specified in paragraph (a) of this section, listed in an information disclosure statement is required to be provided, even if the patent, publication, pending U.S. application or other information was previously submitted to, or cited by, the Office in an earlier application, unless:**
>
> **(1) The earlier application is properly identified in the information disclosure statement and is relied on for an earlier effective filing date under 35 U.S.C. 120; and**
>
> **(2) The information disclosure statement submitted in the earlier application complies with paragraphs (a) through (c) of this section.**
>
> **In order not to supply references along with an information disclosure statement, this application must have relied upon all of the listed other applications for an earlier effective filing date under 35 U.S.C. 120, which this application does not claim priority under 35 U.S.C. 120, copies of the references were required to be submitted.**
>
> **The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the**

requirements based on the time of filing the statement, including all certification requirements. See MPEP § 609(c)(1).

Applicant has enclosed copies of the references cited in the information disclosure statement and requests that the Examiner consider the cited references.

3. Applicant is advised that should claim 4 be found allowable, claim 5 will be objected to under 37 CFR1.75 as being a substantial duplicate thereof. When who claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

The claims have been amended to remove the duplicate claim.

5. Claims 1-24 are rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed invention is directed to executing a "find first bit" instruction which locates a first bit within a data word having a particular state. However, the level of disclosure provided by the specification does not indicate that applicant had possession of the claimed invention. The disclosure of how to actually accomplish this "find first bit" instruction amounts to mere statements that the instruction is executed, and that the bit is found, without providing any details as to how to go about actually implementing the "find" part of "find first bit". For example, see fig. 4 where box 440 simply states "execute the bit operation" without giving any details of how that "execution" is accomplished. Figure 6 contains a blank box 600 containing only the label "find first logic". There is no disclosure of the logic within box 600 which performs the "find first" function, and as the "find first" function of box 600 is critical to performing the claimed instruction operation, it's omission amounts to an indication that the inventors, at time of invention, did not themselves have possession of the requisite logic within box 600 that performs the "find first" function. The written specification is similarly lacking in description of the structure and function of the "find first logic" of box 600. The specification spends seven pages (pg. 6-13) describing basic processor background architecture and yet devotes only 18 lines on page 13 to describing the "find first" aspects of the invention, the description amounting to little more than "the ALU performs the operation". Furthermore, about half of those 18 lines again describe conventional processor architecture techniques amounting to little more than "instructions contain source and destination operand specifier values". On pg. 14, figure 4 is described, and the totality of the description given for box 440 is exactly: "In step 440, the processor executes the bit operation instruction decoded." This simply states that the function is performed (which is merely an inherent statement, because unless it is performed, no operation happens) but provides no details as to how to perform this function. This is further evidence that the inventors did not have possession

of the knowledge of how to perform this function, because had they had possession of this knowledge, they are required by law to disclose it upon filing a patent application. The description of figure 6 begins on line 16 of page 14 and ends at line 13 of page 15. Again the description of box 600, which knowledge of the internal functionality is critical to the invention, is simply:

"When a find first instruction is decoded, the instruction decoder 620 sends control signals to the find first logic to cause the find first logic to perform a masking operation on the value received from the register 330 which in the illustrative embodiment is a 16 bit value. The masking operation performed is determined by the particular type of find first instruction. In general, the masking operation may produce a value of all zeros except for the bit position occupied by the first zero (or one) from the left or right or the first bit change depending on the instruction"

This description states the input to the find first logic receives a 16 bit value, that it performs a mysterious "masking operation", and that it outputs a value having all zero bits except for the particular bit that the instruction was operating upon. However, this description fails to describe how the "masking operation" performs this mysterious feat of consuming a 16 bit quantity and mysteriously outputting a value of all zeros except for the desired bit. Lack of description of this mysterious "masking operation" is further evidence that the inventors did not have possession of this critical element of the invention at the time of filing for a patent.

6. Claims 1-24 are rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As described, supra. in regards to the inventors not having possession of a critical element of the invention at time of filing, this lack of disclosure of how to actually perform the "find first" operation also presents a non enabling disclosure of the invention. Because the description of the "find first" logic amounts to "the logic finds the first bit", one of ordinary skill in the art would be unable to make and/or use the invention because the critical key component necessary to perform the invention has not been disclosed. Without disclosure of the internal operation and function of "find first logic" (600), it is impossible to make and/or use the invention claimed in this application without undue experimentation on the part of one of skill in the art. Therefore, the omission of this critical element of the invention from the application results in a lack of enablement of the claimed invention.

Applicant respectfully disagrees and submits that the application is enabling to one of ordinary skill in the art to practice the invention without undue experimentation. The Examiner states that the disclosure presented is not enabling. The Examiner, however, has cited the Digital VAX11/780 Architecture Handbook ("Digital") and the Intel Pentium Processor Family Developer's Manual Volume 3: Architecture and Programming Manual ("Intel") references as

enabling prior art to make rejections for anticipation and obviousness. Neither the cited portion of Digital nor the cited portions of Intel references contain more disclosure than the present application. Therefore, by the Examiner's reasoning, neither the cited portion of Digital nor the cited portion of Intel are enabling disclosures for use in showing anticipation or obviousness. Applicant respectfully disagrees and argues that Applicant's disclosure is enabling as shown by the level of detail in the Digital and Intel references.

> **7. Claim 8 is rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**
>
> **7.1. The following terms lack proper antecedent basis:**
>
> **7.1.1. "the find first one instruction" claim 8;**

Claim 8 has been withdrawn.

> **14. As to claim 9, Digital taught that the instruction was a find first bit change instruction ("Find First Clear", "Find First Set").**
>
> **15. As to claim 11, Digital taught that the find first bit change instruction finds the first bit change from the right side of a memory location (see figure under "Operation").**

Applicant respectfully disagrees. The cited portion of Digital does not disclose a find first change bit instruction, as required by the claims. For at least this reason, claim 25-30 are patentable over Digital. Applicant respectfully requests that the Examiner allow claims 25-30.

> **19. Claims 4-5, 7-8, 10, 17, 20, and 23 are rejected under 35 USC § 103 as being unpatentable over Digital, as applied to claims 1-3, 6, 9, 11, and 12-13, supra., in view of Intel Pentium Processor Family Developer's Manual, Volume 3, Architecture and Programming Manual, 1995, Intel Corporation.**
>
> **20. As to claims 4-5, 7-8, 10, 17, 20, and 23 Digital did not teach that the instruction operated from the left side of a memory location. However, Intel taught a pair of instruction (pg. 4-12, BSF, BSR) which together implemented scanning for set bits from both the left side and right sides of memory locations (Bit Scan Forward - scans low-to-high (from bit 0 toward the upper bit positions), Bit Scan Reverse - scans high-to-low (from the uppermost bit toward bit 0). It would have been obvious to a person of**

> **ordinary skill in the art at the time the invention was made to have utilized Intel's teachings of scanning for bits from both the left and right sides of a memory word to modify Digital to additionally scan from the left side of a memory location in addition to it's native scanning from the right side of a memory location. One of ordinary skill in the art would have been motivated to provide both from the left and from the right side scanning because doing so provides greater flexibility to the programmer by allowing him/her to setup their data structures in the arrangement they desire, while still allowing easy use of those data structures by simply selecting the correct direction of scanning for location of set/clear bits.**

Pending claims 1, 2, 12-15, and 24 require the limitation of "find[ing] the first zero from the left side of the memory location." Applicant respectfully disagrees that the claims would have been obvious considering Intel and Digital. "It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements." *Arkie Lures, Inc. v. Gene Larew Tackle*, Inc., 119 F.3d 953, 957 (Fed. Cir. 1997). The Examiners cited teaching or motivation of "providing greater flexibility to the programmer," is a result of combining the references. Neither the references nor the Examiner provide any teaching or result to combine Intel and Digital. For this reason, Applicant respectfully requests that the Examiner reconsider his rejection and that the claims be allowed.

SUMMARY

Applicant contends that the claims are in condition for allowance, which action is requested. Applicant has enclosed the appropriate fees with this response. Should any additional fees be required, Applicant requests that the fees be debited from deposit account number 50-1673.

Respectfully submitted,

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